

AMENDMENT AND RESPONSE**PAGE 6**

Serial No.: 10/811,617

Filing Date: March 29, 2004

Attorney Docket No. 125.013US03

Title: BONDED SUBSTRATE FOR AN INTEGRATED CIRCUIT CONTAINING A PLANAR INTRINSIC
GETTERING ZONE**REMARKS**

Applicant has reviewed the Office Action mailed on September 15, 2005 as well as the art cited. Claim 18 has been amended. Claims 1-20 are pending in this application.

Claim Objections

Claim 18 was objected to because of informalities. The Applicant has amended claim 18 to correct typographical errors that lead to the objection. In amending claim 18, no new matter was introduced. In particular, amended claim 18 is support on line 11, page 6 of the present application. Accordingly, the Applicant respectfully requests the withdrawal of the objection of claim 18.

Rejections Under 35 U.S.C. § 102

Claims 1 is rejected under 35 U.S.C. § 102(e) as anticipated by Henley (U.S. Patent No. 6,083,324). To establish a section 102 rejection, a single reference must teach every aspect of the claim either explicitly or inherently. MPEP 706(02).

Claim 1

Independent claim 1 is as follows:

1. (Original) A method of forming a semiconductor device comprising:
implanting ions through a first surface of a monocrystalline semiconductor material to a selected depth forming an amorphous layer adjacent the first surface;
heating the semiconductor material to convert the amorphous layer to a first layer of semiconductor material; and
bonding a handle wafer to the first surface of the semiconductor material.

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The Applicant respectfully traverses the rejection of claim 1. The Henley reference does not teach every aspect in claim 1. For example, as illustrated above, Claim 1 requires implanting into the first surface then bonding a handle wafer to the first surface. Hence the first surface becomes the bottom of the device layer (adjacent the handle wafer). By doing this, no implant damage or contamination knock on ions can occur in the surface region where devices are later formed because the implant never crosses or enters that region. The Henley reference does not teach this aspect. Since the Henley reference does not teach every aspect of claim 1, the applicant respectfully requests the withdrawal of the rejection of claim 1 under section 102.

Double Patenting

Claims 1-20 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-23 of U.S. Patent No. 6,255,195.

Claims 1-9, 11, 12, 19 and 20 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 3 and 16 of U.S. Patent No. 6,825,535.

Applicant has filed, with this response, a terminal disclaimer to overcome the Double Patenting rejection. Accordingly, the Applicant respectfully requests the withdrawal of the Double Patenting rejection of claims 1-20.

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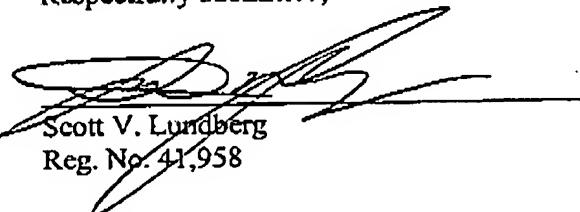
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Title: BONDED SUBSTRATE FOR AN INTEGRATED CIRCUIT CONTAINING A PLANAR INTRINSIC
GETTERING ZONE**CONCLUSION**

Applicant respectfully submits that the claims 1-20 are in condition for allowance and notification to that effect is earnestly requested. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 332-4720, ext. 227.

Please charge any additional fees or credit any overpayments to Deposit Account No. 502432.

Respectfully submitted,

Date: 12-13-08
Scott V. Lundberg
Reg. No. 41,958

Attorneys for Applicant
Fogg and Associates, LLC
P.O. Box 581339
Minneapolis, MN 55458-1339
T - (612) 332-4720
F - (612) 677-3553